Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1–10 (cancelled).

Claim 11 (Currently amended). An arrangement for use in a current controlled oscillator comprising:

a first section providing a first differential output;

a second section providing a second differential output; and

a loading structure electrically connecting the first differential output with the second differential output, the loading structure ~~comprised of~~ including at least one resistive element in series with ~~and~~ at least one reactive element ~~electrically connecting the first differential output with the second differential output, the resistive and reactive elements~~ to form a series combination, the series combination being connected in parallel with a further reactive element, the loading structure having a time constant determined dominantly by the series combination at high control current, the loading structure configured to substantially extend the linear operating frequency range of the current controlled oscillator.

Claim 12 (Previously Presented). The arrangement of claim 11, wherein the first and second section are comprised of at one least parallel connection and at least one series connection of transistors.

Claim 13 (Previously Presented). The arrangement of claim 11, wherein the loading structure includes at least one transistor and at least one capacitor.

Claim 14 (Previously Presented). The arrangement of claim 13, wherein each of the at least one transistors of the loading structure has a gate operably coupled to ground.

Claim 15 (Previously Presented). The arrangement of claim 13, further comprising a power supply rejection ratio compensation section configured to compensate at least partially for variations in power supply voltage, the power supply rejection ratio compensation section operably coupled to at least one gate of the at least one transistor of the loading structure.

Claim 16 (Previously Presented). The arrangement of claim 15, wherein the power supply rejection ratio compensation section, the first section and the second section are powered by the same power supply voltage, and wherein the power supply rejection ratio compensation section includes a diode and a current source.

Claim 17 (Cancelled). ~~The arrangement of claims 13, wherein the loading structure includes a resistive device in series with a capacitive device, the resistive device and the capacitive device both coupled in parallel with a second capacitive device.~~

Claim 18 (Previously Presented). The arrangement of claim 11, wherein the at least one resistive element comprises at least one transistor and the at least one reactive element comprises at least one capacitive element.

Claim 19 (Previously Presented). The arrangement of claim 18, wherein each of the at least one transistors comprises a field effect transistor.

Claim 20 (Previously Presented). The arrangement of claim 19, wherein the field effect transistor comprises a pMOS transistor.

Claim 21 (Currently amended). An arrangement for use in a current controlled oscillator comprising:

a first transistor circuit providing a first differential output;

a second transistor circuit section providing a second differential output; and

a loading circuit ~~including at least a first capacitive element~~ to coupled between the first differential output and the second differential output ~~and a resistive/capacitive series circuit~~

~~coupled between the first differential output with the second differential output~~ comprised of at least one resistive element in series with at least one capacitive element to form a series combination, the series combination being connected in parallel with a further capacitive element.

Claim 22 (Previously Presented). The arrangement of claim 21, wherein each of the first transistor circuit and the second transistor circuit comprises:

first and second parallel transistors coupled in series with a series transistor.

Claim 23 (Currently amended). The arrangement of claim 21, wherein the ~~resistive/capacitive~~ series ~~circuit~~ combination includes at least one transistor and at least one capacitor coupled in series.

Claim 24 (Currently amended). The arrangement of claim 23, wherein each of the at least one transistors of the ~~resistive/capacitive~~ series ~~circuit~~ combination has a gate operably coupled to ground.

Claim 25 (Currently amended). The arrangement of claim 23, further comprising a power supply rejection ratio compensation section configured to compensate at least partially for variations in power supply voltage, the power supply rejection ratio compensation section operably coupled to at least one gate of the at least one transistor of the ~~resistive/capacitive~~ series ~~circuit~~ combination.

Claim 26 (Previously Presented). The arrangement of claim 25, wherein the power supply rejection ratio compensation section includes a diode and a current source.

Claim 27 (Currently amended). The arrangement of claim 21, wherein the ~~resistive/capacitive~~ series ~~circuit~~ combination includes two transistors coupled by a capacitor.

Claim 28 (Cancelled). ~~The arrangement of claim 21, wherein the resistive/capacitive series circuit include at least one transistor and one capacitive element.~~

Claim 29 (Currently amended). The arrangement of claim ~~28~~ 27, wherein each of the at least one transistors comprises a field effect transistor.

Claim 30 (Previously Presented). The arrangement of claim 29, wherein the field effect transistor comprises a pMOS transistor.

Claim 31 (New). An arrangement for use in a current controlled oscillator comprising:

a first section providing a first differential output;

a second section providing a second differential output;

a loading structure comprised of at least resistive element and at least one active element electrically connecting the first differential output with the second differential output, the resistive and reactive elements configured to substantially extend the linear operating frequency range of the current controlled oscillator, wherein the loading structure includes at least one transistor and at least one capacitor, and

a power supply rejection ratio compensation section configured to compensate at least partially for variations in power supply voltage, the power supply rejection ratio compensation section operably coupled to at least one gate of the at least one transistor of the loading structure.

Claim 32 (New). The arrangement of claim 31, wherein the power supply rejection ratio compensation section, the first section and the second section are powered by the same power supply voltage, and wherein the power supply rejection ratio compensation section includes a diode and a current source.

Claim 33 (New). An arrangement for use in a current controlled oscillator comprising:

a first transistor circuit providing a first differential output;

a second transistor circuit section providing a second differential output;

a loading circuit including at least a first capacitive element coupled between the first differential output and the second differential output and a resistive and capacitive series circuit coupled between the first differential output with the second differential output, wherein the resistive and capacitive series circuit includes at least one transistor and at least one capacitor coupled in series, and

a power supply rejection ratio compensation section configured to compensate at least partially for variations in power supply voltage, the power supply rejection ratio compensation section operably coupled to at least one gate of the at least one transistor of the resistive/capacitive series circuit.

Claim 34 (New). The arrangement of claim 33, wherein the power supply rejection ratio compensation section includes a diode and a current source.